IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-29 (Canceled)

30. (Previously Presented) An instruction pipeline in a microprocessor, comprising:

at least one upstream pipeline unit configured to issue each of a series of instructions on one of a plurality of instruction threads;

at least one downstream pipeline unit configured to allocate each of the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued; and

an instruction queue,

wherein:

in a first operating mode, the instruction queue is configured to:

for each of the series of instructions, responsive to receipt of the instruction:

pass the instruction from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of instruction threads on which each of the series of instructions was issued; and

store a copy of the instruction, at least one memory location being dedicated to each of the plurality of instruction threads;

alternate passing the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions was issued when a stall signal is not present on any of the plurality of instruction threads; and

when the stall signal is present on one of the plurality of instruction threads, pass the series of instructions on an other one of the plurality of instruction threads; and

in a second operating mode, the instruction queue is configured to issue to the at least one downstream pipeline unit at least one of the copies on the one of the plurality of instruction threads on which a corresponding at least one of the series of instructions was previously issued.

31. (Currently Amended) The instruction pipeline of claim [[29]] 30, wherein the at least one upstream pipeline unit is configured to determine the one of the plurality of instruction threads on which to issue each of the series of instructions based the availability of resources on each of the plurality of instruction threads.

32. (Canceled)

33. (Currently amended) The ~~method according to~~ instruction pipeline of claim [[32]] 30, ~~further comprising:~~ wherein the instruction queue maintains ~~maintaining~~ a respective pointer for each of the plurality of instruction threads, wherein the step of issuing the at least one copy includes issuing the at least one of the copies from the queue using the respective pointer for the one of the plurality of instruction threads on which the original instruction was issued.

34-36. (Canceled)

37. (Currently amended) The ~~microprocessor according to~~ instruction pipeline of claim [[36]] 30, wherein the at least one upstream pipeline unit includes at least one of a trace cache and a micro-instruction sequencer.

38. (Currently amended) The ~~microprocessor according to~~ instruction pipeline of claim [[36]] 30, wherein the downstream pipeline unit includes an execution unit.

39-41. (Canceled)

42. (Currently amended) The ~~microprocessor according to~~ instruction pipeline of claim [[36]] 30, wherein the instruction queue includes:

a memory device to store copies of received instructions; and

an output multiplexer which is configured, in [[a]] the first mode of operation, to pass the received instructions from the upstream pipeline unit to the downstream pipeline unit, and which is configured, in [[a]] the second mode of operation, to issue at least one of the stored instruction copies.

43. (New) An method of operating an instruction pipeline in a microprocessor, the method comprising:

issuing, by at least one upstream pipeline unit, each of a series of instructions on one of a plurality of instruction threads;

allocating, by at least one downstream pipeline unit, each of the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued;

in a first operating mode of an instruction queue, for each of the series of instructions, responsive to receipt of the instruction

passing the instruction from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of instruction threads on which each of the series of instructions was issued, wherein passing the instruction includes

alternate passing of the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions was issued when a stall signal is not present on any of the plurality of instruction threads, and

when the stall signal is present on one of the plurality of instruction threads, pass the series of instructions on an other one of the plurality of instruction threads,

storing a copy of the instruction, at least one memory location being dedicated to each of the plurality of instruction threads; and

in a second operating mode of the instruction queue, issuing to the at least one downstream pipeline unit at least one of the copies on the one of the plurality of instruction threads on which a corresponding at least one of the series of instructions was previously issued.

44. (New) The method of claim 43, wherein further comprising:

determining the one of the plurality of instruction threads on which to issue each of the series of instructions based the availability of resources on each of the plurality of instruction threads.

45. (New) The method of claim 43, further comprising:

maintaining a respective pointer for each of the plurality of instruction threads, wherein the step of issuing the at least one copy includes issuing the at least one of the copies from the queue using the respective pointer for the one of the plurality of instruction threads on which the original instruction was issued.

46. (New) The method of claim 43, wherein the at least one upstream pipeline unit includes at least one of a trace cache and a micro-instruction sequencer.

47. (New) The method of claim 43, wherein the downstream pipeline unit includes an execution unit.

48. (New) The method of claim 43, wherein the instruction queue includes:

a memory device to store copies of received instructions; and

an output multiplexer which is configured, in the first mode of operation, to pass the received instructions from the upstream pipeline unit to the downstream pipeline unit, and which is configured, in the second mode of operation, to issue at least one of the stored instruction copies.